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Toward Scalable Fabrication of Atomic Wires in Silicon by Nanopatterning Self-Assembled Molecular Monolayers

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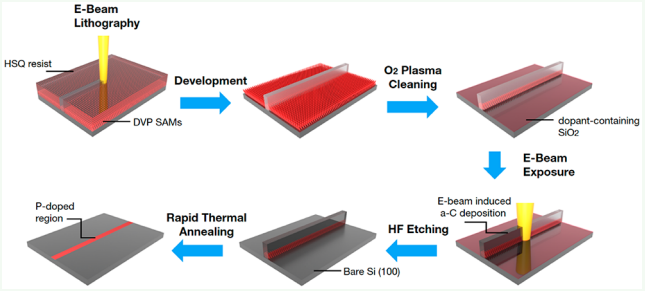
Supporting Information

ABSTRACT: Developing a scalable method to fabricate atomic wires is an important step for building solid-state semiconductor quantum computers. In this work, we developed a selective doping strategy by patterning the self-assembled monolayer to a few nanometers using standard nanofabrication processes, which significantly improves the lateral doping resolution of monolayer doping from microscale to nanoscale. Using this method, we further explore the possibility to fabricate phosphorus wires in silicon by patterning self-assembled diethyl vinylphosphonate monolayers into lines with a width ranging from 500 to 10 nm. The phosphorus dopants are driven into silicon by rapid thermal annealing, forming dopant wires. Four-probe and Hall effect measurements are employed to characterize the dopant wires. The results show that the conductance is linear with the width for the wires, showing the success of the monolayer patterning process to nanoscale. To fabricate atomic wires made of one or a few lines of phosphorus atoms, we need to significantly shorten the thermal diffusion length and increase the dopant incorporation rate at the same time. Pulsed laser annealing may be a promising solution. The present work provides a promising pathway for mass fabrication of atomic wires in silicon that may find important applications in quantum computing.



KEYWORDS: *monolayer doping, nanoelectronics, semiconductors, atomic wires, self-assembled monolayers*

INTRODUCTION

The successful development of complementary metal-oxide-semiconductor (CMOS) technology in the past decades is mainly driven by the constant down-scaling of CMOS transistor sizes.[1] However, the down-scaling has become increasingly difficult as the size of the transistors approaches the physical limit of single atoms.[2,3] Interestingly, Kane proposed in 1998 a new quantum computing device based on the spin coupling of two phosphorus dopant atoms in silicon.[4] A sophisticated quantum computer based on this sort of device requires the precise control of phosphorus atoms at large scale. Simmons et al.[5−8] have demonstrated a scanning tunneling microscopic technique to successfully fabricate atomic wires and single atom transistors in silicon. A Japanese group reported in 2005 a technique to implant single dopant ions into silicon at a spatial resolution of 20 nm.[9] However, these techniques are time-consuming serial processes in which dopants are placed one by one. A parallel process for control of individual dopants at large scale is required if the solid-state semiconductor quantum computing in the coming decades is expected to replicate the success of CMOS technology in the past half-century.

In recent years, self-assembled molecular monolayer doping (MLD) has attracted intensive research interests due to its capability of facilitating mass production, flexibility in doping nonplanar structures, and forming ultrashallow junctions with atomic precision.[10−20] MLD is believed to have a great potential in controllable dopant manipulation at sub-10 nm scale.[13,14,21] However, there is still no general method for effectively patterning a dopant-containing monolayer at nanoscale.

In this work, we first demonstrated a selective doping strategy by patterning self-assembled monolayers (SAMs) to a few nanometers using standard nanofabrication processes, which improves the lateral doping resolution of MLD from microscale[14,16,17] to nanoscale. Using this method, we further explore the possibility of fabricating dopant wires in silicon at large scale. We first grafted a monolayer of diethyl vinylphosphonate (DVP) molecules on intrinsic Si wafer via hydrosilylation. Hydrogen silsesquioxane (HSQ) was used as a negative electron beam resist to pattern the DVP monolayer, forming an array of dopant wires with width from 500 nm down to 10 nm after the phosphorus dopants were thermally driven into silicon by rapid thermal processing (RTP). Four-probe and Hall effect measurements are employed to characterize the dopant wires. The results show that the conductance is linear with the width for the wires, showing the success of the monolayer patterning process to nanoscale. To fabricate atomic wires made of one or a few

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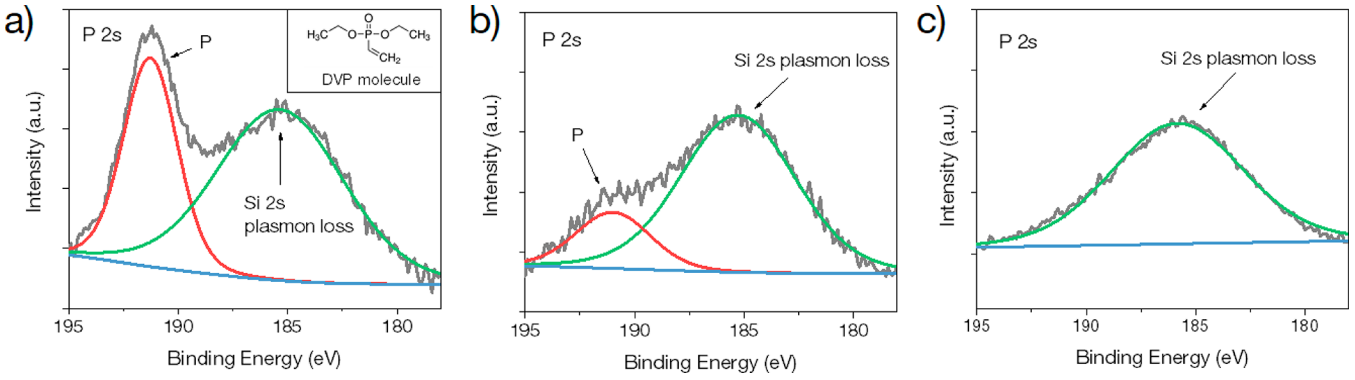

Figure 1. P 2s XPS spectrum acquired from sample (a) of DVP molecules modified, (b) with further treatment with oxygen plasma for 90 s, and (c) after immersion in dilute HF for 1 min.

lines of phosphorus atoms, we need to significantly shorten the thermal diffusion length and increase the dopant incorporation rate at the same time. Pulsed laser annealing may be a promising solution.

RESULTS AND DISCUSSION

We first grafted a monolayer of DVP molecules on intrinsic silicon wafers (>10000 Ω cm). Then electron-beam lithography was used to fabricate an HSQ mask on a DVP-functionalized substrate and define the doping region. For nanopatterning of DVP monolayer, the unprotected DVP monolayer needs to be removed while leaving the HSQ protected region intact. We found an effective way to remove the SAMs via oxygen plasma followed by HF etching (see Experimental Section for details). X-ray photoelectron spectroscopy (XPS) was used to analyze the assembled molecular monolayers on the silicon surfaces after each of the following three sequential steps: (a) self-assembly of DVP monolayers; (b) oxidization of the SAMs by oxygen plasma; (c) removal of organic residue by HF wet etching. Figure 1a shows the P 2s XPS spectrum obtained from the sample grafted with DVP monolayers. The broad bump around 185 eV is ascribed to silicon plasmon loss.[22] The strong peak around 192 eV is attributed to P−O bonds, suggesting that a high concentration of DVP molecules has been successfully immobilized onto the silicon substrate. After oxygen plasma treatment, the P 2s peak shown in Figure 1b is greatly reduced, but still clearly visible. Considering the detection limit of XPS is around 0.1 at. %, the visible P 2s peak indicates that a considerable amount of phosphorus still exists on the silicon surfaces after oxygen plasma treatment. Clearly, oxygen plasma alone is not effective in removing dopant-containing molecular monolayers, as indicated in a previous report.[14] This observation is reasonable, since phosphorus oxide generated during oxygen plasma process is involatile. After the oxygen plasma, treatment of dilute HF solution completely removed the P 2s peak (Figure 1c), indicating the successful removal of phosphorus-related compounds.

The XPS observations were further confirmed by electrical measurements. All three samples were prepared and went through the RTP process (RTP-Table, Premtek Inc.) at 1050 °C for 120 s, as described in Table 1. A 200 nm thick Al film was thermally evaporated onto the four corners of the samples after proper cleaning and HF treatment (see Experimental Section). The van der Pauw measurements were conducted to probe the sheet resistance of these samples. The results were summarized in Table 1. The sheet resistant of P-doped substrate was

Table 1. Sheet Resistances Measured by van der Pauw Technique

sample	R_S (kΩ/□)
1. surface functionalized with DVP	2.0
2. surface functionalized, O_2 plasma 90 s, 1 wt% HF 1 min	260.8
3. control sample (annealed without any surface modification)	252.1

measured to be 2 kΩ/□, indicating the success of the whole MLD process. The secondary ion mass spectroscopy (SIMS) shows that a relatively high concentration of phosphorus has diffused into the silicon substrate as shown in Supporting Information (SI) Figure S1. The P concentration reaches an order of 10^{18} cm^{-3} near the Si surface and drops by 1 order of magnitude in the next 80 nm below the surface. For the sample that was functionalized with DVP monolayers but treated with oxygen plasma and HF etching, the sheet resistance went up to 260.8 kΩ/□, which is comparable to the sheet resistance of the control sample. It suggests that the combination of oxygen plasma and HF etching can completely remove phosphorus from a functionalized surface.

The dopant wires in silicon were fabricated following the procedure illustrated in Figure 2. DVP monolayers were first grafted on the intrinsic silicon wafers (>10000 Ω cm) that were cleaned properly (see Experimental Section for details). Electron beam resist HSQ (XR-1541-002, Dow Corning) was used to create patterns that protect part of the self-assembled DVP monolayers from being oxidized by oxygen plasma, since HSQ will turn into amorphous SiO_2 after electron beam exposure. As demonstrated previously, HF etching can completely remove the unprotected DVP monolayers that were treated with oxygen plasma. However, HF will also attack the HSQ SiO_2 at the same time. To increase the resistance of the HSQ SiO_2 against HF etching, a second time of high dosage exposure was performed on the HSQ SiO_2. The high dosage electron beam exposure induced a thin amorphous carbon layer covering the HSQ SiO_2 which protected the underneath SiO_2 and DVP molecules from being attacked by HF (see SI section 1).[23,24]

RTP was then applied to drive the patterned phosphorus dopants into silicon, forming dopant wires in silicon. Each dopant wire connects a pair of the contact pads which were pre-ion-implanted with phosphorus dopants at a concentration of 10^{19} cm^{-3} to facilitate the formation of ohmic contacts with Al electrodes. The device structure is illustrated in Figure 3a. The inserted SEM image shows a 10 nm wide HSQ line after the

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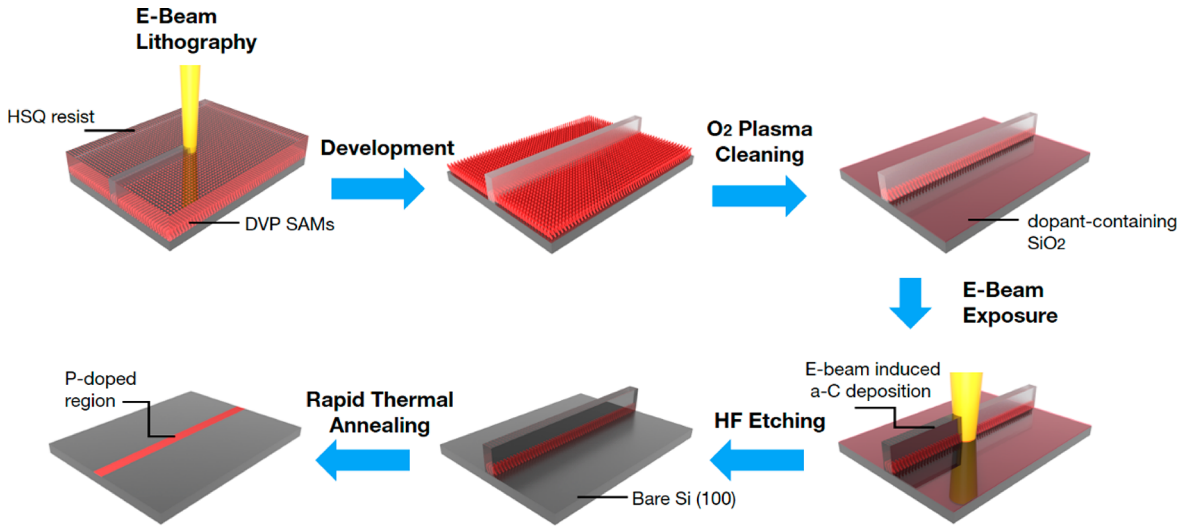

Figure 2. Process flow of the proposed doping strategy.

second e-beam exposure and HF etching. An optical microscopic image of the fabricated dopant-wire array is shown in Figure 3a as well. Each dopant wire is in contact with four micropads for four-probe measurements.

Figure 3b shows the current vs voltage (*IV*) characteristics for the dopant wires at 77 K. The P dopants were driven from the molecular monolayer into the silicon substrate at 1050 °C for 90 s, forming these dopant wires. The width of the dopant wires varies from 500 to 10 nm. Four-probe measurements were also conducted at 77 K, showing that the contact resistance is negligibly small in comparison with the resistance of the dopant wires. All of the dopant wires show ohmic current−voltage characteristics, indicating that the doping process was successful (Figure 3b). The conductances of the wires at room temperature (RT) were also measured. At RT, the conductivity of the intrinsic silicon substrate is relatively high. To eliminate the influence of the substrate, a control device was made on the same substrate that went through the whole fabrication process except the self-assembly of DVP monolayers on silicon surface. The conductance of the dopant wires at RT were found by deducting the control conductance from the total wire device conductance. Figure 3c exhibits the width dependence of the wire conductance measured at 77 K (blue) and RT (red).

At RT, the nanowire conductance linearly decreases as the wire narrows down to 15 nm, projecting to zero conductance at zero width. From the linear correlation, we found that the sheet resistance of the wires is 0.95 kΩ/□ at RT. (Note that the sheet resistance of the wires is lower than that of the monolayer film doping in Table 1. This is likely because the high dose of electron beam exposure induces a high concentration of vacancies that increase the incorporation rate of phosphorus dopants.[25,26]) When the temperature is lowered to 77 K, the situation is more complicated. For wires wider than 80 nm, the conductance shows a linear dependence on wire width and the sheet resistance is calculated to be 1.40 kΩ/□. It is well-known that the ionization rate of phosphorus dopants in nondegenerate silicon will reduce by approximately 1 order of magnitude when the temperature is lowered from RT to 77 K unless the doped silicon is degenerate due to high doping concentration. This small difference in sheet resistance between RT and 77 K indicates that the wires wider than 80 nm are at least partly degenerate. Indeed, as shown in Figure 3d for the 500 nm wide wire, the conductance saturates to 1.8 μS instead of dropping to zero as the temperature is lowered to 2 K, indicating that the dopant wire is partly in metallic state. The relatively large drop in conductance is because most phosphorus dopants diffuse deep in silicon, forming a relatively low doping concentration. Only a thin layer of silicon near the surface (a few nanometers thick) is highly doped and in metallic state. Electrons in this thin layer of metallic silicon may behave like a two-dimensional gas. We applied a strong magnetic field perpendicular to the silicon surface. As shown in Figure 3e, the magnetoresistance increases abruptly at 1.10, 3.85, and 5.40 T, probably due to the quantum Hall effect.

For those wires narrower than 40 nm, the nanowire conductance also shows a linear correlation with wire width but the slope is much smaller (inset in Figure 3c), indicating that the dopant wires may completely transit to nondegeneracy due to the reduction of the P doping concentration. The sheet resistance for those narrower wires is found to be 13.90 kΩ/□ at 77 K. The measured sheet resistance decays by about 1 order of magnitude compared to the RT value, which further indicates the nondegeneracy of these narrower wires. The reduction of the P doping concentration is caused by the dopant thermal diffusion when the diffusion length is comparable to half of the wire width (lateral diffusion toward both sides). This phenomenon can be analytically described by the following "source-limited" diffusion model.[27] In the cross-section perpendicular to the wire axial direction, the x-coordinate is pointing to the silicon bulk from the silicon surface and the y coordinate is along the silicon surface. The origin is set at the center of the wire. The diffusion source is located at $x = 0$ and $-w/2 \le y \le w/2$, where w is the source width. Suppose the DVP monolayer as the dopant source has a surface dopant concentration of N_0 atoms/cm^2. The diffusion profile $C(x,y,t)$ in $x-y$ coordinates is the superposition of all point sources located within $(-w/2, w/2)$ at $x = 0$. Given the diffusion coefficient D at a certain temperature and the diffusion time t, the diffusion profile can be written as the following eq 1, according to the source-limited diffusion model.[27]

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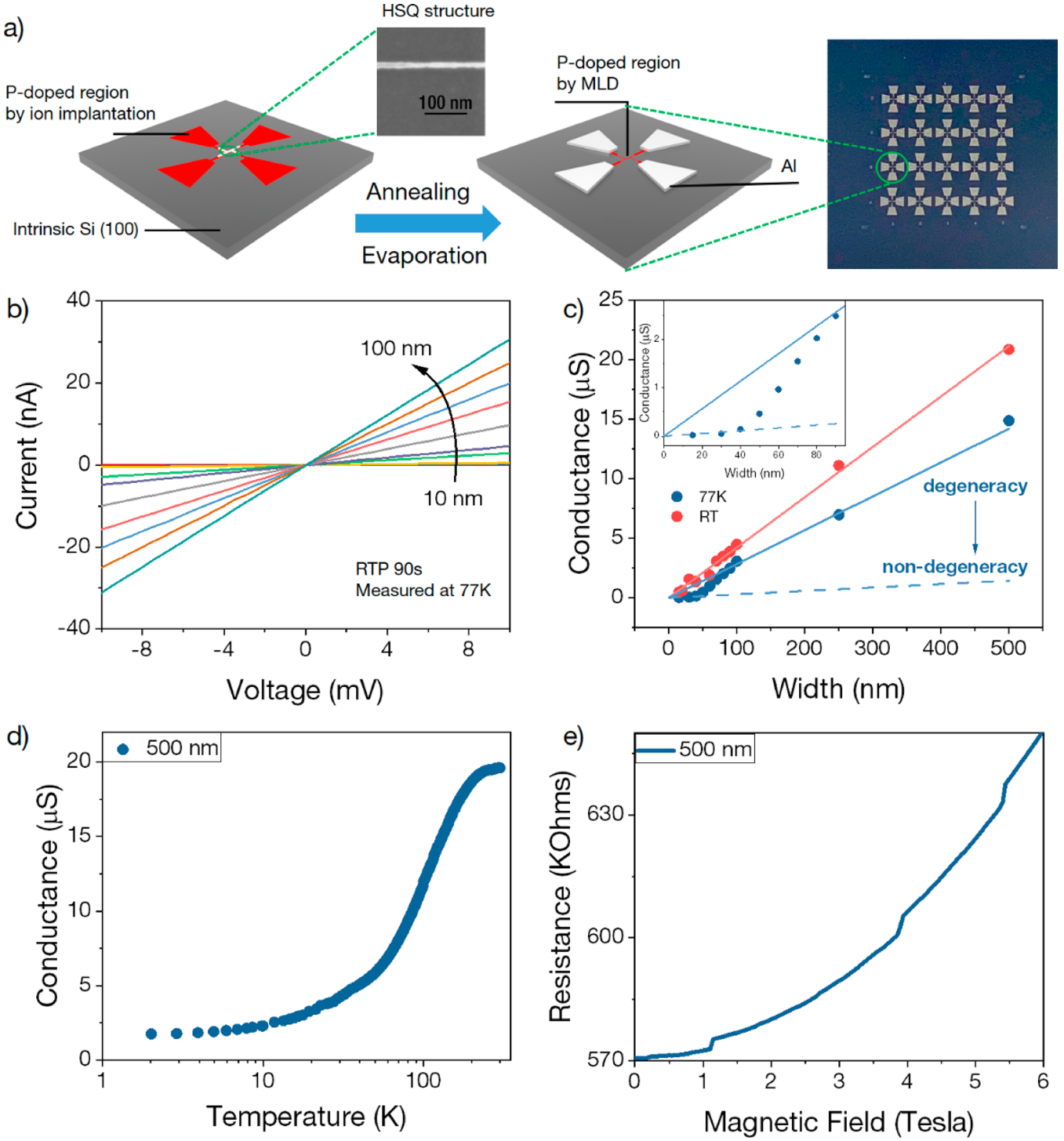

Figure 3. (a) Illustration of device structure and fabrication process. (b) Two probe measurements at 77 K of $I-V$ curves of dopant-wire devices with width ranging from 10 to 100 nm. (c) Conductance of dopant-wire devices as a function of width ranging from 15 to 100 nm, measured at RT and 77 K. (d) Conductance of dopant wire with a width of 500 nm as a function of temperature, plotted on a semilog scale. (e) Magnetoresistance of 500 nm wide dopant wire at 2 K.

$$C(x, y, t) = K\int_{-w/2}^{w/2} e^{-(x^2+(y-y')^2)/4Dt}\, dy' = \sqrt{\pi Dt}\, K e^{-x^2/4Dt}\left[\mathrm{erf}\left(\frac{y+\frac{w}{2}}{2\sqrt{Dt}}\right) - \mathrm{erf}\left(\frac{y-\frac{w}{2}}{2\sqrt{Dt}}\right)\right] \quad (1)$$

where K is a normalization factor. Clearly, for a certain diffusion time, the peak concentration is located at the center of the dopant line $C(x,0,t) = 2\sqrt{\pi Dt}\, K e^{-x^2/4Dt}\, \mathrm{erf}\left(\frac{w}{4\sqrt{Dt}}\right)$. When w is large enough, $\mathrm{erf}\left(\frac{w}{4\sqrt{Dt}}\right) \to 1$ and $C(x,0,t) \to \frac{N_0}{\sqrt{\pi Dt}} e^{-x^2/4Dt}$ according to the doping profile of the one-dimensional source-limited diffusion model. Clearly, we have $K = \frac{N_0}{2\pi Dt}$.

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In this case, the doping profile of dopant wire can be rewritten as eq 2

$$C(x, y, t) = \frac{N_0}{2\sqrt{\pi Dt}} e^{-x^2/4Dt} \left[\text{erf}\left(\frac{y + \frac{w}{2}}{2\sqrt{Dt}} \right) - \text{erf}\left(\frac{y - \frac{w}{2}}{2\sqrt{Dt}} \right) \right] \quad (2)$$

The conductance R^{-1} can be expressed as

$$R^{-1} = \frac{1}{l} \int_{-\infty}^{\infty} \int_{0}^{\infty} q\mu C(x, y, t)\, dx\, dy = \frac{q\mu N_0}{l} w \quad (3)$$

where l is the wire length equal to 25 μm as designed. Equation 3 shows that the conductance R^{-1} should have a linear correlation with line width w at RT, consistent with the experimental data in Figure 3c. The slopes of the fitted lines are proportional to the product of electron mobility and surface dose (μN_0), which are summarized in Table 2. Similarly, eq 3 can be applied to the wires wider than 80 nm at 77 K, from which μN_0 can be also found.

Table 2. Surface Dose N_0 Extracted from Figure 3c for Wires Wider Than 80 nm

		μN_0	N_0 (cm^{-2})
RTP 90 s	RT	6.6×10^{15}	4.2×10^{13}
	77 K	4.5×10^{15}	1.8×10^{13}

At 77 K, the conductance of wide wire is mainly contributed by the degenerate region with a doping concentration larger than 3×10^{18} atoms/cm^3. Previous reports[28,29] show an electron mobility around 250 cm^2/(V s) at 77 K for impurity concentration ranging from 3×10^{18} to 1×10^{19} atoms/cm^3; then the surface dose N_0 should be around 1.8×10^{13} atoms/cm^2. Given the empirical correlation of mobility with doping concentration at RT,[10,30] the equivalent surface dose N_0 at RT is found to be $\sim 4.2 \times 10^{13}$ atoms/cm^2 (see SI section 2), as shown in Table 2. This indicates that approximately 60% of dopants diffused deep into the silicon (tens of nanometers), forming lightly doped nondegenerate Si.

In Figure 3c, we observed the conductance deviates from the linear correlation at the line width of ~80 nm, implying that the conductance of the degenerate silicon begins to become less dominant. Figure 4a shows the modeling results for dopant wires with different diffusion length (see SI section 3 for details). Clearly, the modeling conductance is quite close to experimental results when $\sqrt{Dt} = 31.5$ nm. For a diffusion length of ~31.5 nm and annealing time of 90 s, the diffusion coefficient is calculated to be 1.1×10^{-13} cm^2/s. Considering the empirical formula of phosphorus diffusivity in silicon can be expressed as[31]

$$D = 0.79 \exp\left[-\frac{(3.29/\text{eV})}{kT} \right]$$

The calculated diffusion coefficient at 1050 °C is 2.45×10^{-13} cm^2/s, quite close to the value 1.1×10^{-13} cm^2/s that we estimated from the diffusion length of ~31.5 nm. Figure 4b plots the surface dopant concentration profile $C(0,y,t)$ for a constant diffusion length $\sqrt{Dt} = 31.5$ nm, where

$$C(0, y, t) = \frac{N_0}{2\sqrt{\pi Dt}} \left[\text{erf}\left(\frac{y + \frac{w}{2}}{2\sqrt{Dt}} \right) - \text{erf}\left(\frac{y - \frac{w}{2}}{2\sqrt{Dt}} \right) \right]$$

is a function of lateral position y and line width w. Clearly, the maximum dopant concentration located at $C(0,0,t)$ and this concentration is proportional to $\text{erf}\left(\frac{w}{4\sqrt{Dt}} \right)$. As w gets closer to the diffusion length $\sqrt{Dt}$, the maximum concentration will significantly drop below the critical concentration ($=3 \times 10^{18}$ cm^{-3}), turning the partly degenerate Si into complete nondegeneracy. In Figure 4b, the critical width is around 50 nm, which is consistent with experimental results.

Atomic wires can be regarded as wires made of one or a few lines of controlled active atoms. To make atomic wires, in our case the e-beam resist HSQ needs to be patterned with a width well below 10 nm to cover one or a few lines DVP molecules. This goal is achievable by optimizing resist and substrate thickness, since we have already realized 10 nm wide monolayer patterning with 50 nm thick resist using the proposed method. However, the diffusion process creates randomness in the spatial distribution of dopant atoms, which is not desirable in

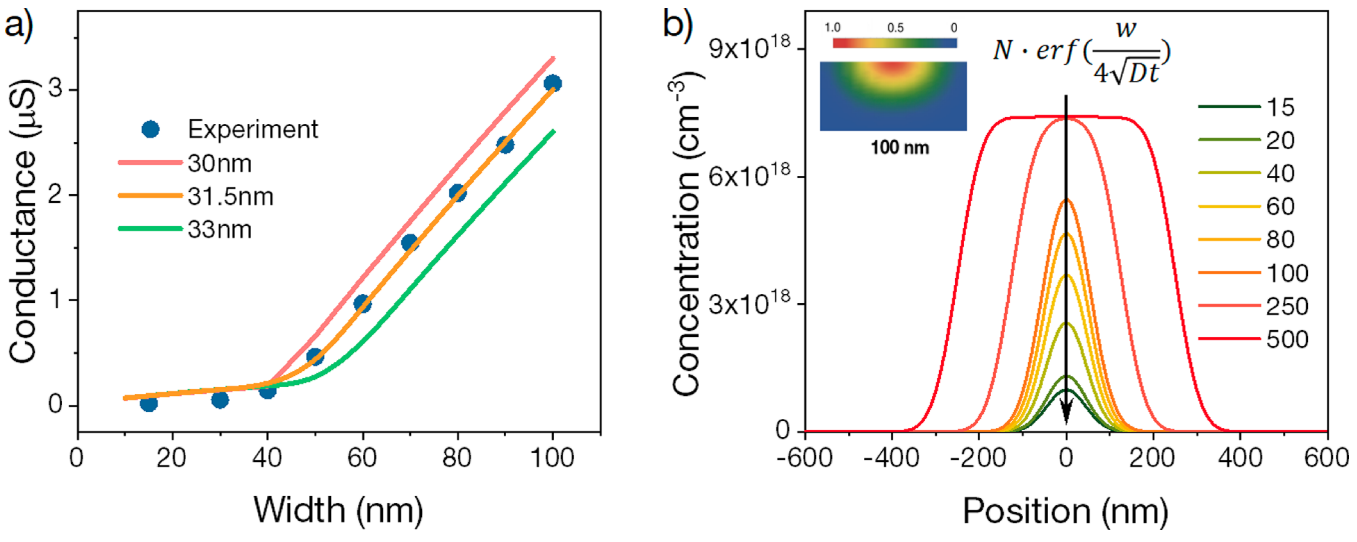

Figure 4. (a) Experimental data and modeling conductance for dopant wires with diffusion lengths of 30, 31.5, and 33 nm. (b) Surface concentration plotted as a function of lateral position and line width with diffusion length of 31.5 nm.

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fabrication of atomic wires. The diffusion length of 31.5 nm will make all dopant atoms out of control as the width of dopant source gets closer to or even smaller than the diffusion length (lateral diffusion toward both sides of wires). Clearly, we need to significantly reduce the diffusion length to several atomic layers to fabricate atomic wires by shortening the period of high temperature annealing. However, this has exceeded the processing capacity of the commonly used RTP method. When the annealing time is shortened from 90 to 30 s, the number of phosphorus dopants diffusing into silicon is greatly reduced (see SI section 4), meaning that only part of the dopants in the source are incorporated into silicon. This creates randomness in the number of dopants in the wire per unit length, which may lead to high non-uniformity or even discontinuity in atomic wires. While fabricating atomic wire is beyond our existent experimental capabilities, we believe that pulsed laser annealing is the most promising tool for atomic wire fabrication by nanopatterning SAMs.

CONCLUSION

In this work, we successfully developed a strategy for patterning SAMs at 10 nm scale. Phosphorus dopant wires with a width ranging from 500 to 10 nm were fabricated by nanopatterning of DVP monolayer and RTP. The diffusion length of the dopants is approximately 30 nm. Linear dependence of conductance on width at RT indicates the success of the selective doping process, albeit a deviation of conductance from the linear dependence is observed at low temperature when wire width is comparable to two times the diffusion length. To fabricate atomic wires made of one or a few lines of atoms, pulsed laser annealing should be used to shorten the thermal diffusion length to several atomic layers and increase the dopant incorporation rate close to 100%. The present work provides a promising pathway for scalable fabrication of atomic wires in silicon that may find important applications in quantum computing.

EXPERIMENTAL SECTION

Monolayer Formation. Nearly intrinsic silicon wafer (4 in., (100)-oriented, 525 ± 25 μm thick, resistivity > 10 kΩ cm) was cleaved into 1.5 cm by 1.5 cm pieces and ultrasonicated with acetone, ethanol, and DI water for 3 min each to remove organic residue. After being rinsed with DI water, the sample was immersed into piranha solution (H_2SO_4:H_2O_2 = 3:1) at 120 °C for 60 min. The cleaned substrate was then rinsed with DI water and dried under nitrogen flow.

The surface functionalization of hydrogen-terminated silicon with DVP via thermal hydrosilylation have been well-studied, as described elsewhere.[32,33] DVP (>98%, TCI Shanghai) was first diluted with 1,3,5-trimethylbenzene (>97%, TCI Shanghai) at a ratio of 1:12 in a glovebox under Ar atmosphere, followed by deoxygenation using Ar bubbling. The cleaned substrate was etched in 2.5% HF solution for 90 s to form a hydrogen-terminated surface. After being quickly rinsed with DI water and dried under argon flow, the substrate was transferred into the DVP solution. The hydrosilylation process was conducted at 160 °C for 12 h using a heating jacket under Ar atmosphere. The obtained sample was then cleaned with acetone, ethanol, and DI water in a sonication bath for 3 min each to remove any physisorbed molecules.

Patterning of Self-Assembled Monolayers. HSQ (XR-1541-002, Dow Corning) resist was applied by spin-coating on a preformed monolayer on substrate with a thickness around 50 nm, followed by prebaking at 90 °C for 60 s. The line structures with width ranging from 10 to 500 nm was directly written into the HSQ resist on the designed position, using a Vistec EBPG-5200+ electron-beam lithography system. Exposure was done at 100 keV acceleration voltage, beam current of 0.3 nA, with a dose of 3000 μC/cm^2. The substrate was then developed in 2.38% tetramethylammonium hydroxide (TMAH) solution for 1 min and copiously rinsed with DI water. After that, the dried sample was treated with oxygen plasma for 90 s, for the complete decomposition of the exposed molecular monolayer. To improve the wet etching resistance of HSQ resist, a second exposure was conducted on the obtained HSQ structure before the HF etching process, with a dose of 190 mC/cm^2. The double exposed sample was dipped in 1 wt% HF solution for 1 min, gently rinsed with DI water, and dried under nitrogen flow.

Silicon Oxide Deposition and Thermal Annealing. A thin layer of silicon oxide was applied on the silicon substrate by spin-coating of IC1-200 (Futurrex Inc. USA), as previously described.[12,15] RTP was performed at 1050 °C for 90 s, with a ramp temperature of 100 °C/s. After annealing, the silicon oxide capping layer was removed by immersing the substrate in a buffer oxide etchant (BOE) solution (HF:NH_4F = 6:1, CMOS grade; J. T. Baker Co. USA) solution for 20 min.

Electrical Characterizations. Photolithography and thermal evaporation of aluminum were performed to make electrical contract to the ion implantation area of dopant-wire devices. Electronical measurement was performed on a cryogenic probe station (Model TTPX, Lake Shore Cryotronics, Inc., USA) at 77.6 K. A Keysight B1500A semiconductor device parameter analyzer was used to generate and collect voltage/current data.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.9b00749.

SIMS data, fabrication details on second e-beam exposure, additional AFM images, FTIR, surface dose calculation, conductance modeling at 77 K, and electrical measurement results on dopant wire annealed at 1050 °C for 30 s (PDF)

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Notes

The authors declare no competing financial interest.

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