Gold Mask-Assisted Fabrication of Contamination-Free Monolayer MoS_2 Transistors

Yumeng Liu, Yizhuo Wang, Zhengfang Fan, Jianyong Wei, Seyed Saleh Mousavi Khaleghi, Shuwen Guo, Zhentao Lian, Hao Wei, Zhijuan Su, *Member, IEEE*, Rui Yang, *Member, IEEE*, Robert Kudrawiec, and Yaping Dan, *Senior Member, IEEE*

***Abstract*— Atomically thin MoS_2 is a promising material for field-effect transistors (FETs) and electronic devices. However, traditional photolithographic processes introduce polymeric photoresist contamination to 2-D materials, leading to a large uncertainty in their electrical property. In this work, we demonstrate a novel fabrication method using gold as a mask for patterning and etching, which protects 2-D materials from contamination of polymeric photoresists. This technique enables the fabrication of clean monolayer MoS_2 transistors with Ohmic contacts. MoS_2 devices was mass-produced using both traditional photo-lithography (TPL) and gold mask lithography (GML). Statistics (∼200 devices) shows that MoS_2 devices produced by TPL vary in electrical properties by three orders of magnitude, while those fabricated by GML are highly reproducible with the conductivity variance within one order of magnitude.**

***Index Terms*— Gold mask lithography (GML), MoS_2, ohmic contact, Raman spectrum.**

Received 12 November 2024; revised 5 January 2025; accepted 19 February 2025. This work was supported in part by the Oceanic Interdisciplinary Program of Shanghai Jiao Tong University under Grant SL2022ZD107; in part by Shanghai Pujiang Program under Grant 22PJ1408200; in part by the National Science Foundation of China (NSFC) under Grant 62304131, Grant W2412118, and Grant 92364107; in part by Shanghai Jiao Tong University Scientific and Technological Innovation Funds under Grant 2020QY05; and in part by the Science and Technology Commission of Shanghai Municipality (STCSM) under Grant 23QA1405300 and Grant 24ZR1491500. The review of this article was arranged by Editor Y. Xu. *(Corresponding authors: Zhijuan Su; Yaping Dan.)*

Yumeng Liu and Zhengfang Fan are with the University of Michigan–Shanghai Jiao Tong University Joint Institute, Shanghai 200240, China, and also with the Department of Micro/Nano Electronics, School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China.

Yizhuo Wang, Jianyong Wei, Zhentao Lian, Rui Yang, and Yaping Dan are with the University of Michigan–Shanghai Jiao Tong University Joint Institute, Shanghai 200240, China (e-mail: yaping.dan@sjtu.edu.cn).

Seyed Saleh Mousavi Khaleghi is with the University of Michigan–Shanghai Jiao Tong University Joint Institute, Shanghai 200240, China, and also with the Department of Electrical and Electronic Engineering, University of Melbourne, Melbourne, VIC 3010, Australia.

Shuwen Guo is with the School of Energy and Materials, Shanghai Polytechnic University, Shanghai 201209, China.

Hao Wei is with the Department of Micro/Nano Electronics, School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China.

Zhijuan Su is with the Global Institute of Future Technology, Shanghai Jiao Tong University, Shanghai 200240, China (e-mail: zhijuan.su@sjtu.edu.cn).

Robert Kudrawiec is with the Department of Semiconductor Materials Engineering, Wroclaw University of Science and Technology, 50-370 Wroclaw, Poland.

Digital Object Identifier 10.1109/TED.2025.3547294

I. Introduction

TWO-DIMENSIONAL semiconducting materials, such as transition metal dichalcogenides (TMDs), have emerged as a promising candidate to potentially replace silicon for next-generation integrated circuits [1], [2], [3], [4], [5], [6], [7]. However, their adoption to semiconductor manufacturing has been hindered by several challenges, in particular the widely used photolithography process. Traditional photolithography (TPL) is a polymeric process in which a thin layer of photoresist residue is often left on the 2-D material's surface [8], [9], [10]. This residue cannot be effectively removed by conventional solvents and may result in poor metal-semiconductor contacts, leading to significant performance degradation [11], [12]. For bulk semiconductors, such residues can be removed using harsh cleaning processes, such as oxygen plasma etching [8], [13]. However, these methods are unsuitable for atomically thin 2-D materials, as they can cause damage to the material's atomic layers [14], [15], [16], [17], further compromising the quality of the metal–semiconductor interface. Consequently, the presence of photoresist residue leads to substantial variability in device performance, which poses a significant barrier to the mass production of 2-D material-based integrated circuits. This issue makes the commercialization of 2-D materials for high-volume applications challenging, as the devices exhibit inconsistent electronic characteristics.

To address this challenge, we propose a novel fabrication method that employs gold as a protective mask for atomically thin 2-D materials during the photolithographic process. This technique effectively prevents the 2-D materials from being contaminated by photoresists, thereby ensuring pristine metal-semiconductor contacts. While other methods, such as selective etching [18], [19] or wet chemical cleaning [20], have been suggested to tackle contamination, they are either not

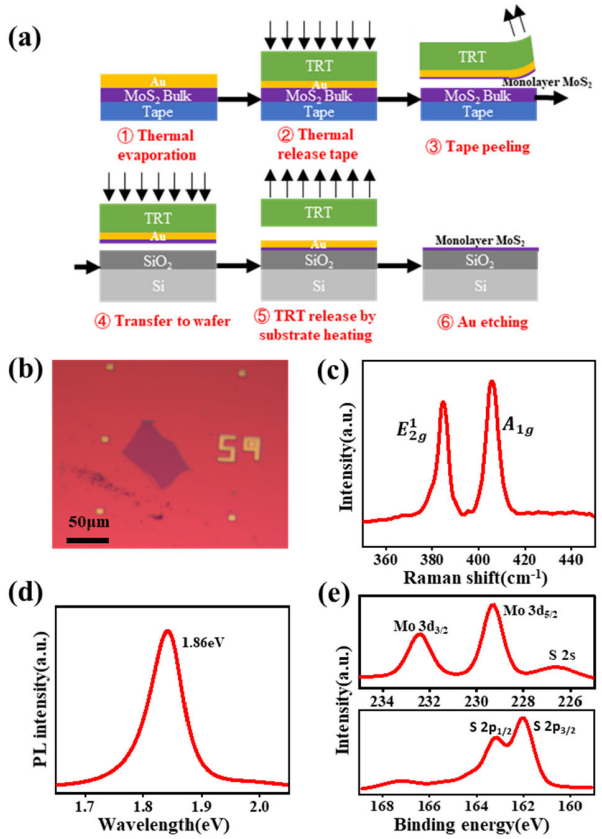

Fig. 1. (a) Device process for the gold-assisted exfoliation to fabricate monolayer MoS_2 TRT is short for thermal release tap. (b) Optical image of the monolayer MoS_2. (c) Photoluminescence spectrum of MoS_2 under green laser excitation ($\lambda = 532$ nm). (d) Raman spectroscopy of MoS_2. (e) XPS of Mo 3d (top panel) and S 2p (bottom panel) spectra for MoS_2.

scalable or fail to maintain the pristine interfaces necessary for high-performance devices. In contrast, our gold mask lithography (GML) method is simple, scalable, and compatible with existing photolithography equipment, making it suitable for industrial applications and large-area production of 2-D material-based devices.

Through this innovative approach, we successfully fabricated MoS_2 transistors with pristine metal contacts, achieving highly reproducible electrical characteristics. We conducted large-scale fabrication using both TPL and GML. The statistics shows that the devices fabricated by TPL exhibit a variance of three orders of magnitude in conductance, whereas those fabricated by GML have a conductance variance within an order of magnitude. The results highlight the stability of this metal mask technique introducing contamination-free 2-D material transistors. The ability to fabricate high-quality, clean interfaces with minimal contamination is poised to make significant contributions to electronic device manufacturing and integration, paving the way for more sophisticated and efficient 2-D material-based technologies.

II. Results and Discussion

A gold-assisted exfoliation technique was employed to exfoliate monolayers from bulk MoS_2 [21], as illustrated in Fig. 1(a). Initially, a thin layer of gold was thermally evaporated onto the fresh surface of a bulk crystal MoS_2 piece. Gold atoms will preferentially bond with the surface sulfur atoms. The Au-S bonds are significantly stronger than the Van der Waals forces among MoS_2 layers, thereby facilitating the selective exfoliation of the top layer using thermal release tape (TRT). The tape was subsequently transferred to a target substrate (SiO_2/Si). The assembly was heated on a hotplate, followed by mild O_2 plasma treatment to remove any residual adhesive. The O_2 plasma power and etching duration were carefully controlled to prevent damage to the underlying monolayer MoS_2 during the etching process. Finally, the gold film was selectively etched using a KI/I_2 solution, which effectively removes the gold without affecting the MoS_2.

The resultant MoS_2 monolayer is presented in Fig. 1(b). The monolayer nature of the MoS_2 was rigorously verified through advanced spectroscopic techniques. Raman spectroscopy provided definitive evidence of the monolayer status, indicated by a characteristic 18 cm^{-1} peak separation between the E_{2g} and A_{1g} vibrational modes-a hallmark of monolayer MoS_2 [see Fig. 1(c)]. This peak separation aligns with values reported in the literature, further confirming the successful isolation of a single MoS_2 layer [22].

Moreover, photoluminescence spectroscopy offered additional verification of the monolayer, revealing a prominent photoluminescence peak at 1.86 eV [see Fig. 1(d)] consistent with the direct bandgap of monolayer MoS_2 [23]. This result underscores the high optical quality and uniformity of the exfoliated material. To complement these findings, X-ray photoelectron spectroscopy (XPS) was employed to analyze the chemical states and bonding environments of the MoS_2 [see Fig. 1(e)]. These results collectively validate the successful fabrication of a high-quality and large-area MoS_2 monolayer [21].

Fig. 2(a) depicts the fabrication process for the metal mask technique used with MoS_2. A 40 nm-thick layer of gold was thermally re-evaporated onto the exfoliated MoS_2, followed by the spin coating of a photoresist. The photoresist made contact exclusively with the gold layer, avoiding direct interaction with the MoS_2. Standard photolithography was employed to pattern the photoresist. Gold etching was performed using a KI/I_2 solution, which selectively etched the gold without affecting the MoS_2 monolayer. The temperature-dependent I–V characteristics (from 80 to 300 K), presented in Fig. 2(b), demonstrate an increase in current with rising temperature. The results indicate the presence of a strong Schottky barrier between the gold contact and MoS_2. The gate transfer characteristic curve at room temperature shown in Fig. 2(c) reveals the n-type transistor behavior of the MoS_2, with a hysteresis attributed to defects and other nonideal factors [24], [25]. The inset is the optical microscopic image of the device. Additionally, for the semiconductors that have a low carrier mobility like MoS_2 monolayers, the Schottky junction is best described by the diffusion model [26], [27]. In this model, the saturation current at reverse bias is proportional to electric field intensity and the exponential term of Schottky barrier height $e^{-(q/k_BT)\Phi_B}$

$$I_{ds} = AA_{2D}^{**}\exp\left[-\frac{q}{k_BT}\left(\Phi_B - \frac{V_{ds}}{n}\right)\right] \quad (1)$$

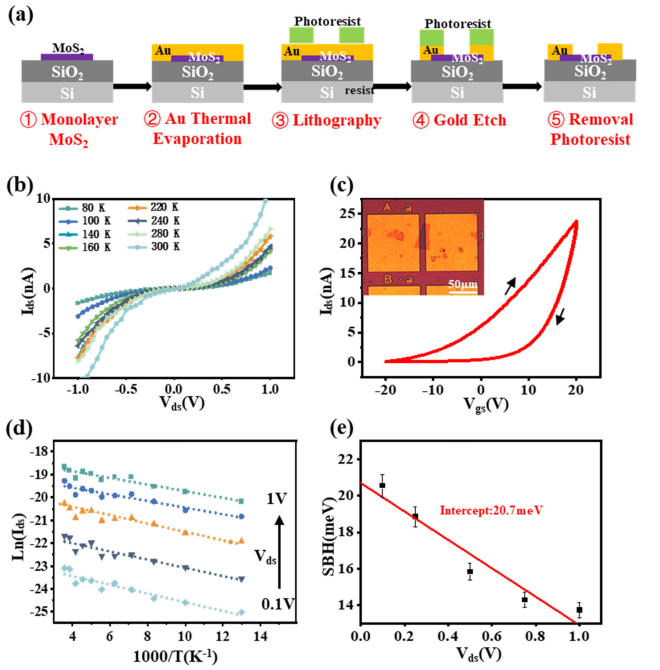

Fig. 2. (a) Fabrication process for MoS_2 devices with pure gold electrode contact. (b) *I*–*V* curves at different temperatures. (c) Gate transfer characteristics of the MoS_2 transistor (inset: device optical microscopic image). (d) Linear fit of ln (I_{ds}) versus 1000/T. (e) Slopes extracted from the linear fit is plotted as a function of V_{ds} and Φ_B is derived from its *y*-intercept.

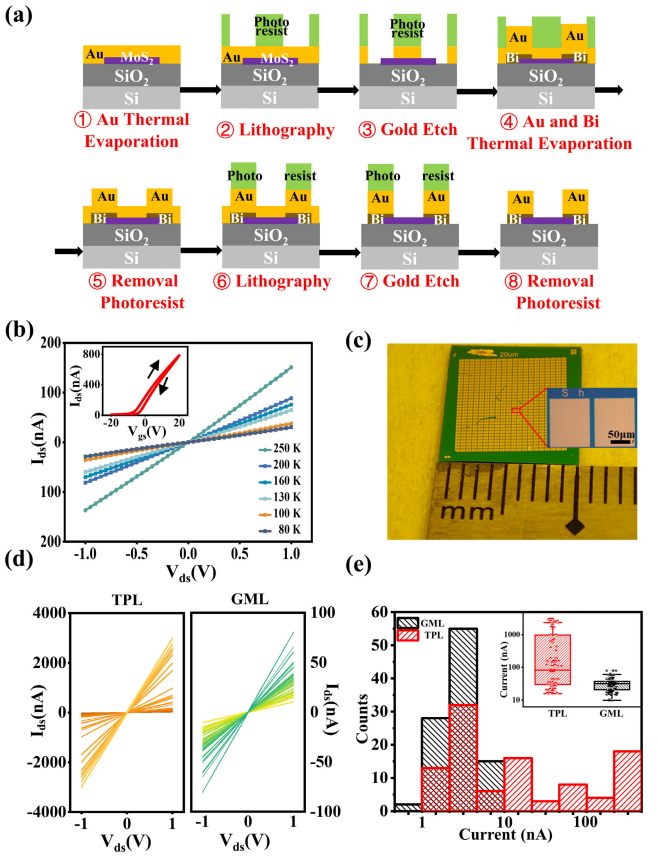

Fig. 3. (a) Fabrication process for MoS_2 devices with bismuth and gold electrode contacts. (b) *I*–*V* curves at different temperatures (inset: gate transfer characteristics of the MoS_2 transistor). (c) Optical microscope image of device array fabricated by GML, along with a magnified view of a single device. (d) *I*–*V* curves of traditional photo-lithography (TPL) and GML for 100 devices. (e) Current statistics of the device fabricated by classical photolithography and our gold masked lithography.

where A represents the contact area, A_{2D}^{**} represents the effective 2-D equivalent Richardson constant which is temperature independent, q denotes the magnitude of the electron charge, k_B is the Boltzmann's constant, Φ_B refers to the Schottky barrier height, n is the ideality factor, and V_{ds} is the source-drain bias.

Following (1), we have $\ln(I_{ds}) = \ln(AA_{2D}^{**}) - (q/k_BT)(\Phi_B - (V_{ds}/n))$. Therefore, it is not surprising that the current I_{ds} in Arrhenius plot is linear with 1000/T under different source-drain bias (V_{ds}) as shown in Fig. 2(d). The slope of these linear lines can be extracted from the experimental data in Fig. 2(d). Theoretically, the slope is given by $(q/k_B1000)(\Phi_B - (V_{ds}/n))$. The bias-dependent barrier height $\Phi_B - (V_{ds}/n) = (k_B1000/q) \times$ slope is replotted in Fig. 2(e). Clearly, the bias-dependent barrier height is linearly correlated with V_{ds}. Extending the linear correlation to intersect with the *y*-axis will obtain the Schottky barrier height Φ_B which is 20.7 $\pm$ 0.2 meV.

For MoS_2-based integrated circuits, it is crucial to have highly reproducible devices in Ohmic contacts [28], [29], [30]. Bismuth, known for its low melting point and semimetallic characteristics, is a suitable metal to form Ohmic contacts with the MoS_2 monolayer [31]. It is well known that polymeric photoresist residues are often left on the surface of 2-D semiconductors in TPL [10]. These residues may change the conductance of the MoS_2 channel and create unreliable contacts with metals. Here, we take the advantage of the process developed for clean MoS_2-metal contacts and demonstrate a new paradigm to create clean contacts of MoS_2 with metals other than Au.

As shown in Fig. 3(a), gold was first thermally evaporated onto the 2-D material surface, followed by the spin coating of photoresist. Photolithography and metal etching were subsequently performed. The pattern in the photoresist are transferred to the protecting gold film. The desired metal films (Bi and Au in our case) were then evaporated to contact the 2-D materials. The remaining metal films were removed in the following lift-off process. Photolithography with a pattern complementary to the previous pattern was performed to protect the desired metal films from subsequent gold etching. Throughout the entire processes, MoS_2 remained clean without direct contact with photoresist.

Fig. 3(b) presents the current–voltage (I–V) characteristics of the device measured at different temperatures. In comparison with the I–V characteristics shown in Fig. 2(b), the device exhibits a linear I–V relationship from room temperature down to 80 K, indicating the formation of a high-quality Ohmic contact. Since Ohmic contact has been established, the Schottky barrier is completely eliminated, and the current is mostly governed by the channel resistance [32]. As a result, the Arrhenius plot cannot be used to extract the Schottky barrier height. The consistent linearity of the I–V curves under different thermal conditions further demonstrates the

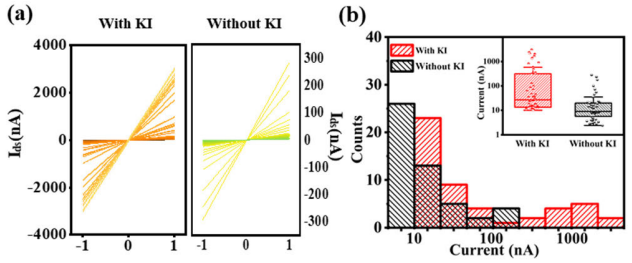

Fig. 4. (a) *I*–*V* curves treated with and without KI for 50 devices. (b) Current statistics of the device fabricated with and without KI.

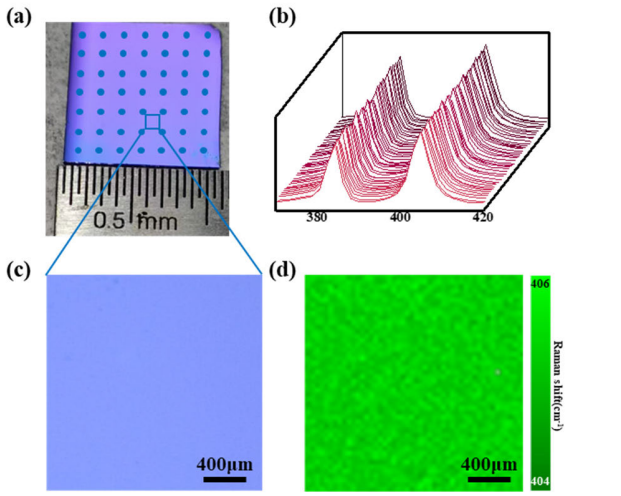

Fig. 5. (a) MoS_2 monolayer synthesized on a SiO_2/Si substrate. The marked dots are where Raman spectra are taken. (b) Raman mapping spectra from different locations marked in (a). (c) Optical microscope image of a 2 mm region arbitrarily selected from the sample. (d) Raman mapping of the A_{1g} peak of MoS_2 within the region shown in (c).

stability and reliability of the contact interface, highlighting the effectiveness of the fabrication process in achieving optimal electrical performance. The inset is the gate transfer characteristics of the MoS_2 transistor, showing that the MoS_2 channel is n-type. The narrow hysteretic loop indicates that the defects in these MoS_2 devices are significantly suppressed.

To make the above observations statistically meaningful, we fabricated 100 Au/Bi contact MoS_2 devices with GML. For comparison, we also fabricated another 100 Au/Bi contact MoS_2 devices with TPL. All of the devices were fabricated with identical geometries and electrode thicknesses on MoS_2 monolayers synthesized by chemical vapor deposition [33], [34], [35] (Six Carbon, Inc., Shenzhen, China). Fig. 3(c) shows the optical image of the MoS_2 device array on the chip. The inset shows the optical microscopic image of one such device.

Fig. 3(d) presents *I*–*V* curves of 100 devices fabricated separately by TPL and GML. Fig. 3(e) shows the statistics of the currents in darkness at a constant bias of 1 V applied across the devices. The inset is a box plot of the data, displaying the interquartile range (IQR) from the 25th to the 75th percentiles, with the central line representing the median. The current of the devices produced by TPL varies from device to device in a range of three-orders-of-magnitude. This large uncertainty is attributed to the uncontrollable doping effects of the photoresist residues chemically or electrically. In contrast, the currents of the devices produced by GML concentrate within one order of magnitude at ∼tens of nA. Clearly, the GML effectively mitigates the doping effect of the photoresist residue, thereby enhancing the reproducibility and reliability of device performances. These devices are fabricated in the cleanroom with the Class 100 000 which means 100 000 particles per cubic meters in the air space of the cleanroom. We believe that the variation from device to device fabricated by GML will be much smaller if these devices are fabricated in a lower-class cleanroom (Class 100, for instance).

However, in addition to the potential doping effect of organic photoresists on 2-D materials, the KI solution may also introduce doping [36]. To exclude the impact of KI/I_2 doping, we have included data from KI-treated devices for comparison. Two batches of devices were fabricated using TPL, ensuring identical processing conditions, with one batch soaked in a KI/I_2 solution for 5 s prior to fabrication (the same duration used for gold etching in the previous process). Fig. 4(a) shows the *I*–*V* curves for 50 devices with and without KI treatment, and Fig. 4(b) presents the corresponding statistical data. It is observed that KI treatment results in slight doping of the devices, but does not improve the current variability.

On the other hand, to exclude the possibility that the three-order-of-magnitude variation in current comes from the inhomogeneity of the synthesized MoS_2 monolayers, we conducted a uniformity test on the monolayer MoS_2 used for the study in Fig. 3. Fig. 5(a) shows the optical image of the monolayer MoS_2 sample. The MoS_2 monolayer is synthesized on SiO_2/Si substrate with a size of 1 × 1 cm. We chose 49 points to test the uniformity of the MoS_2 monolayer by performing Raman spectroscopy [see Fig. 5(b)]. The Raman spectra indicate that the MoS_2 monolayer is globally uniform. To assess the local uniformity of the MoS_2 monolayer, we selected a 2 mm region of the MoS_2 sample for Raman mapping. The optical image of this region is shown in Fig. 5(c), and the corresponding A_{1g} peak Raman mapping is presented in Fig. 5(d). The slight fluctuations are attributed to measurement errors. These results consistently demonstrate that the MoS_2 exhibits excellent uniformity, and that the three-order-of-magnitude variation observed for the devices fabricated by TPL originates from the process itself instead of the nonuniformity in MoS_2 monolayer.

III. Conclusion

In this work, we successfully developed a novel fabrication process for monolayer MoS_2 transistors, utilizing gold as a protective mask during the patterning and etching stages. This technique effectively mitigates contamination from photoresists and other organic solvents, preserving the pristine condition of the MoS_2 surface and ensuring high-quality metal contacts. As a result, the fabricated transistors exhibit Ohmic contacts and robust electrical performance in reproducibility and uniformity. This advancement not only significantly enhances the performance and reliability of MoS_2-based transistors but also establishes a benchmark for contamination-free fabrication of 2-D material devices.

By enabling consistent, contamination-free fabrication, this technique opens the door to the scalable manufacturing of high-performance 2-D material-based electronics and optoelectronics. As it is compatible with existing photolithography process and scalable for large-area production, this approach holds promise for transforming the commercial viability of 2-D materials and paving the way for their widespread adoption in next-generation semiconductor technologies.

Acknowledgment

The MoS_2 monolayers were characterized at the Instrumental Analytical Center, Shanghai Jiao Tong University.

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